查询XRT8020供应商

650 MHZ CLOCK & CRYSTAL MULTIPLIER WITH LVDS OUTPUTS

NOVEMBER 2003 *REV. 1.0.2*

DESCRIPTION

The XRT8020 is a monolithic analog phase locked loop that provides a high frequency LVDS clock output, using a low frequency crystal or reference clock. It is designed for SONET/SDH and other low jitter applications.The high performance of the IC provides a very low jitter LVDS clock output up to 650 MHz, while operating at 3.3 volts. The XRT8020 has a selectable 8x, 16x or 32x internal multiplier for an external crystal or signal source. The Output Enable pin provides a true disconnect for the LVDS output. The very compact (4 x 4 mm) low inductance package is ideal for high frequency operation.

APPLICATIONS

- Gigabit Ethernet
- SONET/SDH
- SPI - 4 Phase 2
- 8x, 16x or 32x Clock Multiplier for Computer and Telecommunication Systems

FEATURES

- 575 MHz to 675 MHz operating range
- Low Output Jitter: 9ps rms typical at 622 MHz
- On Chip Crystal Oscillator Circuit
  - Optimized for 15 to 40 MHz crystals
  - Uses parallel fundamental mode crystal
- Selectable 8x, 16x or 32x multiplier
- Selectable ÷ 1 or ÷ 2 LVDS output
- LVDS output meets TIA/EIA 644A Specification (2001)
- 3.3V ±10% Low power CMOS: 80 mW typical
- -40°C to +85°C operating temperature
- Extremely small 16-lead QFN package

FIGURE 1. BLOCK DIAGRAM OF THE XRT8020

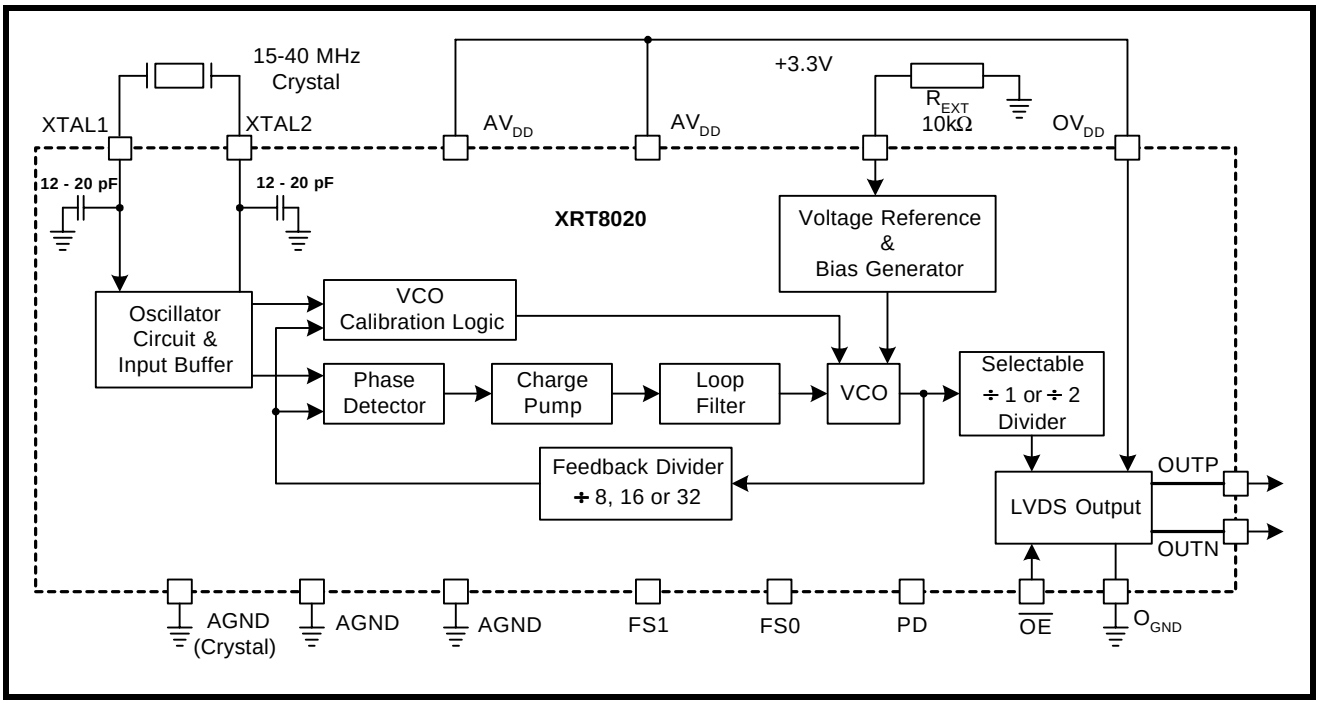
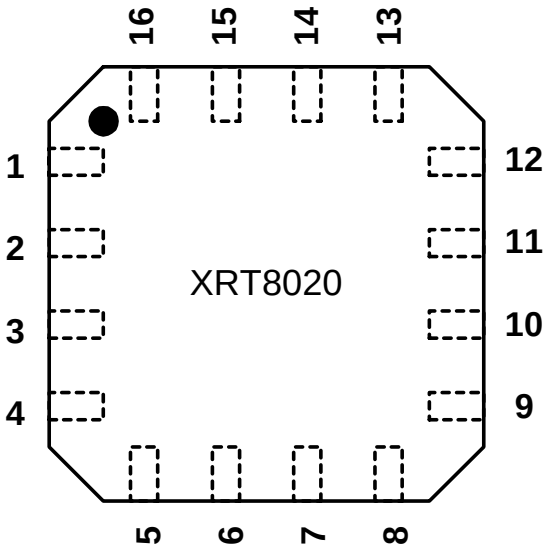


FIGURE 2. XRT8020 PIN LOCATION - (TOP VIEW)



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT8020IL	16 - Pin QFN	-40°C to +85°C

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PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AVDD		3.3V ±10% Analog Supply for Crystal Oscillator
2	AGND		Analog Ground for Crystal Oscillator
3	XTAL1	I	Crystal pin 1 or external clock input
4	XTAL2	O	Crystal pin 2 (output drive for crystal)
5	AGND		Analog Ground
6	REXT	I	External Bias Resistor (10KΩ to ground)
7	$\overline{OE}$	I	Output Enable, Active low (*Internal 50KΩ pull-down to ground*)
8	PD	I	Power Down, Active High *(Internal 50KΩ pull-down to ground)*
9	FS1	I	Frequency select "1" *(Internal 50KΩ pull-down to ground)*
10	FS0	I	Frequency select "0" *(Internal 50KΩ pull-up to VDD)*
11	AGND		Analog Ground
12	OGND		Output Ground for LVDS outputs
13	OUTN	O	LVDS negative output for 50Ω line
14	OUTP	O	LVDS positive output for 50Ω line
15	OVDD		3.3V ±10% Digital Supply for LVDS Output buffer
16	AVDD		3.3V ±10% Analog Supply

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.5 to 6.0 V
V_{IN}	-0.5 to 6.0 V
Storage Temperature	-65°C to + 150°C
Operating Temperature	-40°C to + 85°C
ESD	>2,000 volts
REXT (±1%)	10kΩ

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply current	I_{DD}		25	30	mA	VDD = 3.3V
Power Save Current	I_{DD}			6	mA	VDD = 3.3V, PD = 1, OEB = 0
Input Digital High	V_{INH}	2.0			V	Pins 7, 8, 9, 10
Input Digital Low	V_{INL}			0.8	V	Pins 7, 8, 9, 10
Crystal Frequency		15		27	MHz	See Section 2.0 for Crystal Selection

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Crystal Frequency		27		40	MHz	See Section 2.0 for Crystal Selection
Clock Input Frequency		72		85	MHz	AC Coupled (FS0=1, FS1=1)
Power on Calibration time				5	ms	After VDD reaches 2.8V ***NOTE:*** *Calibration time = 16,000 clock cycles*
Max Frequency Out	F_{OUT}	575		675	MHz	624 MHz nominal F_{OUT} (See Table 1)
Max Frequency Out	F_{OUT}	285		340	MHz	312 MHz nominal F_{OUT} (See Table 1)
Rise time	T_R		350		ps	CL = 5pF, RL = 100Ω, (20% - 80%)
Fall Time	T_F		350		ps	CL = 5pF, RL = 100Ω, (20% - 80%)
Duty cycle		45		55	%	LVDS output
Differential Output Skew			10		ps	See Figure 3
Output Loading			100		Ω	
Output Voltage Swing	V_{OUT}	250		450	mV	Magnitude of (OUTP-OUTN)
Common Mode Voltage	V_{CM}	1.0	1.2	1.4	V	
Output Short Circuit Current			-5.7	-10	mA	Current limit to ground, V_{DD} or Vp to Vn
Cycle-to-Cycle Jitter			3		ps	rms, at 624 MHz
Cycle-to-Cycle Jitter			3		ps	rms, at 312 MHz
Accumulated Jitter			12		ps	rms, at 624 MHz
Accumulated Jitter			12		ps	rms, 312 MHz
Input Referenced Jitter			9		ps	rms at 622 MHz, See Figure 4
Input Referenced Jitter			9		ps	rms at 312 MHz, See Figure 4

FIGURE 3. LVDS OUTPUT WAVEFORMS AND TEST CIRCUITS

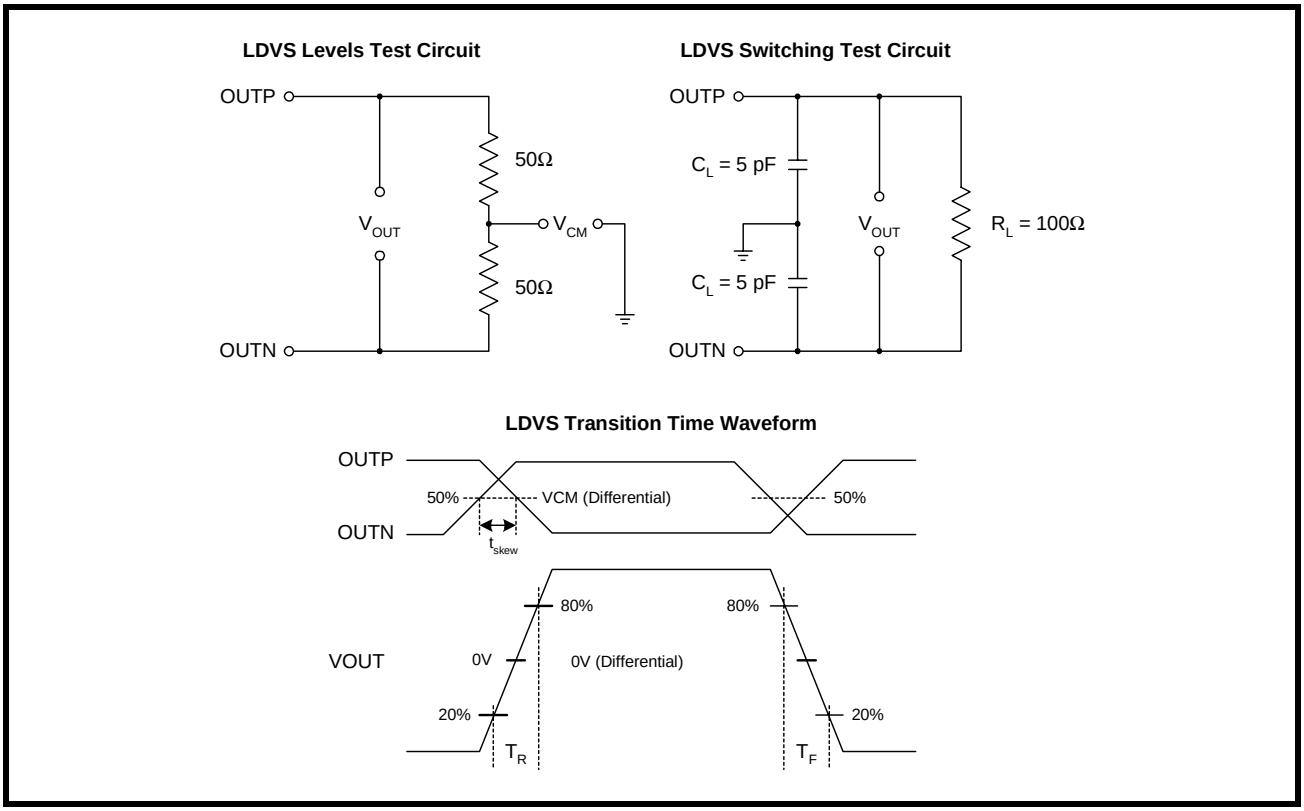


TABLE 1: FREQUENCY SELECTION TABLE

FS0 PIN 10	FS1 PIN 9	CRYSTAL OR CLOCK FREQUENCY	INTERNAL CAPACITOR	MULTIPLY RATIO	OUTPUT DIVIDE	OUTPUT FREQUENCY
1	1	78.0 MHz Clock	NA	8x	1	624 MHz
0	1	39.0 MHz	12 pF	16x	1	624 MHz
1	0	19.5 MHz	20 pF	32x	1	624 MHz
0	0	19.5 MHz	20 pF	32x	2	312 MHz

NOTES:

1. *Use Parallel Fundamental mode crystal*
2. *FS0 has an internal 50KΩ pull-up resistor to VDD*
3. *FS1 has an internal 50KΩ pull-down resistor to GND*

TABLE 2: POWER-DOWN AND OUTPUT TRI-STATE SELECTION TABLE

PD PIN 8	$\overline{OE}$ PIN 7	STATUS	*NOTES:*
1	X	Outputs tri-stated and chip Powered-down	1. *"X" = Don't care* 2. *PD and $\overline{OE}$ have an internal 50KΩ pull-down resistor to ground.*
0	1	Output tri-stated	

1.0 CALIBRATION

The XRT8020 synthesizer jitter performance is optimized by calibration of its Voltage Controlled Oscillator (VCO) upon initial power application. This power ON calibration procedure is automatic and completely transparent to the user. It is initiated automatically upon first application of VDD. In order to bring the center frequency of the VCO close to the desired output frequency, the VCO bias current is adjusted via a current DAC at initial power application. The center frequency of VCO is checked against input reference frequency and calibrated internally to the desired output frequency value. These bias voltage trim bits are then held in latches for as long as the VDD is held above 2.7V (minimum specified operational value of VDD). The user should note following important facts about this calibration procedure for proper operation of the XRT8020:

- For proper operation of the chip and to achieve lowest jitter, the user should follow layout guidelines as described in the User Guide.
- An input crystal of appropriate frequency should be connected at XTAL1 and XTAL2 pins before power is applied to the chip.
- All VDD pins should be tied to 3.3V ±10% simultaneously.
- The power supply should turn on without bouncing below 2.0V smoothly to its specified value in no more than 50msec.
- The calibration takes place during VDD ramp up between 2.6V to 3V values. Once the VDD reaches and maintains 3.0V, the chip retains the calibrated VCO bias voltages in internal latches for proper operation.
- To change a widely different value of crystal or input reference frequency, it is recommended to power down the chip by bringing VDD to 0V and restarting after the change in frequency has occurred.

2.0 CRYSTAL SELECTION

It is recommended that a Fundamental Mode Crystal be used as the timing reference of the XRT8020. The following part has been qualified by EXAR:

CITIZEN Quartz Crystals

20 MHz : HCM49-20.000MABJT

40 MHz : HCM49-40.000MABJT

3.0 DATA AND PLOTS

All plots were recorded using the following parameters and test setup:

- VDD = 3.3 V
- 2” 100Ω Differential Transmission Lines (from LVDS outputs to receiver inputs)
- Fundamental Mode Crystal of 20 MHz
- Vref = 1.5 V (PECL Receiver)

FIGURE 4. INPUT REFERENCED JITTER CONNECTION DIAGRAM

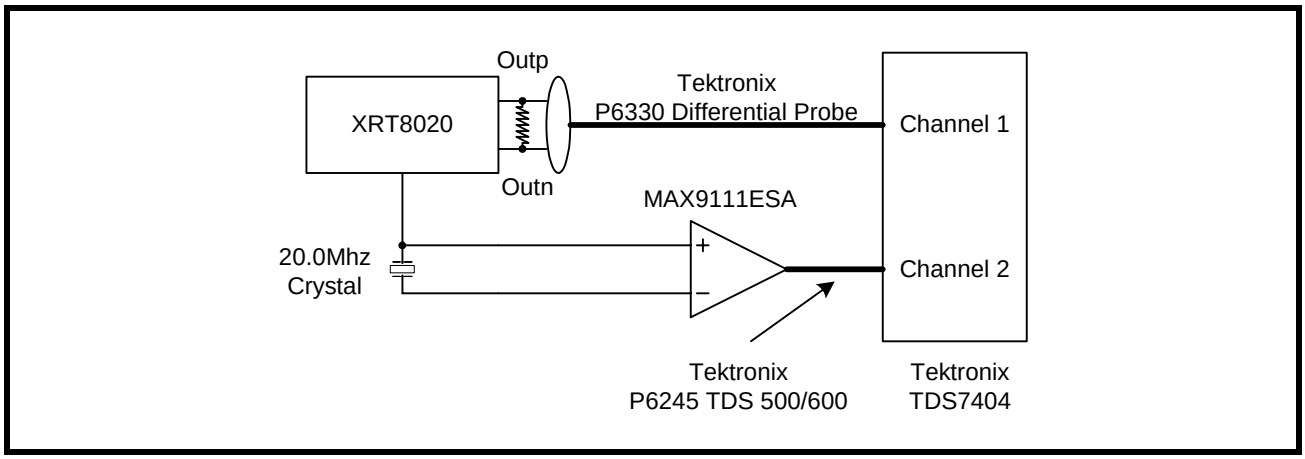


FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF THE XRT8020 AND PECL RECEIVER

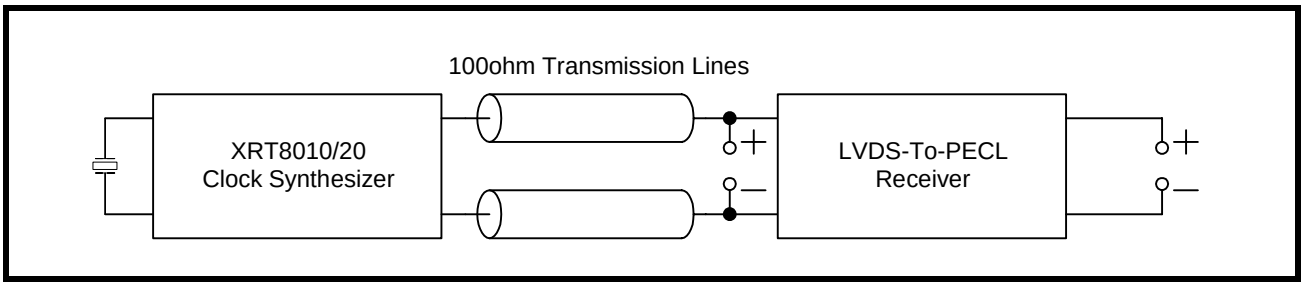


FIGURE 6. LVDS DIFFERENTIAL OUTPUT

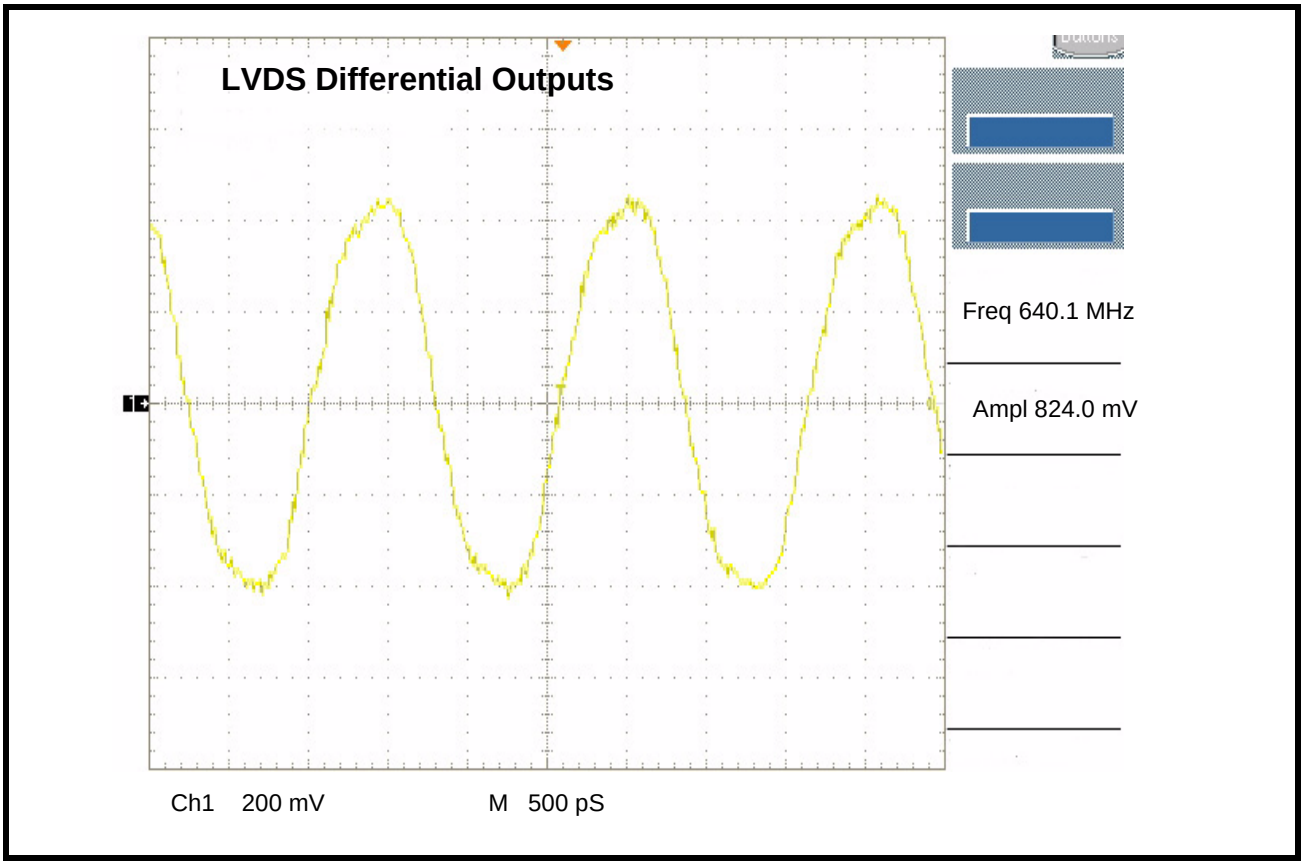


FIGURE 7. PECL DIFFERENTIAL OUTPUT

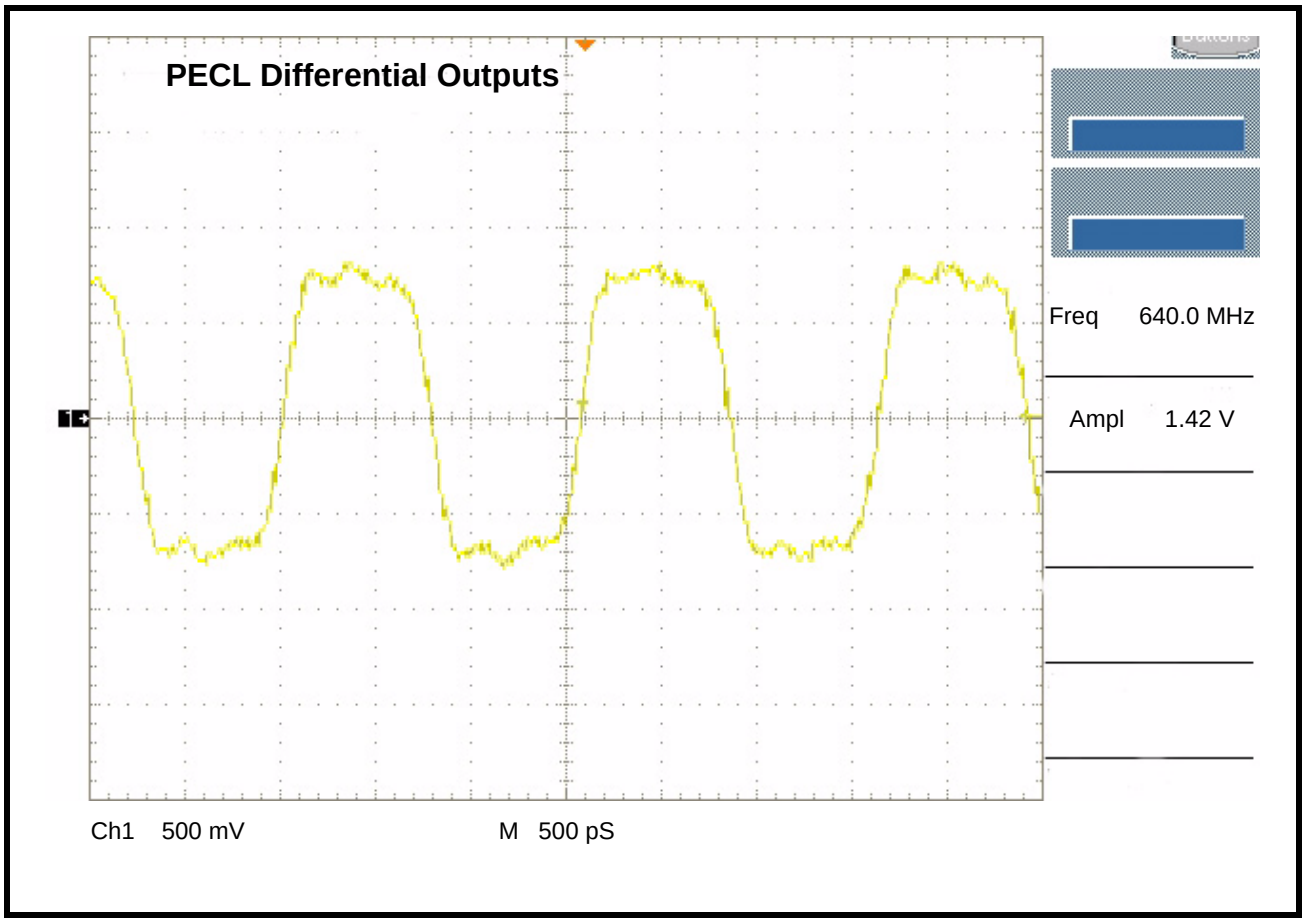
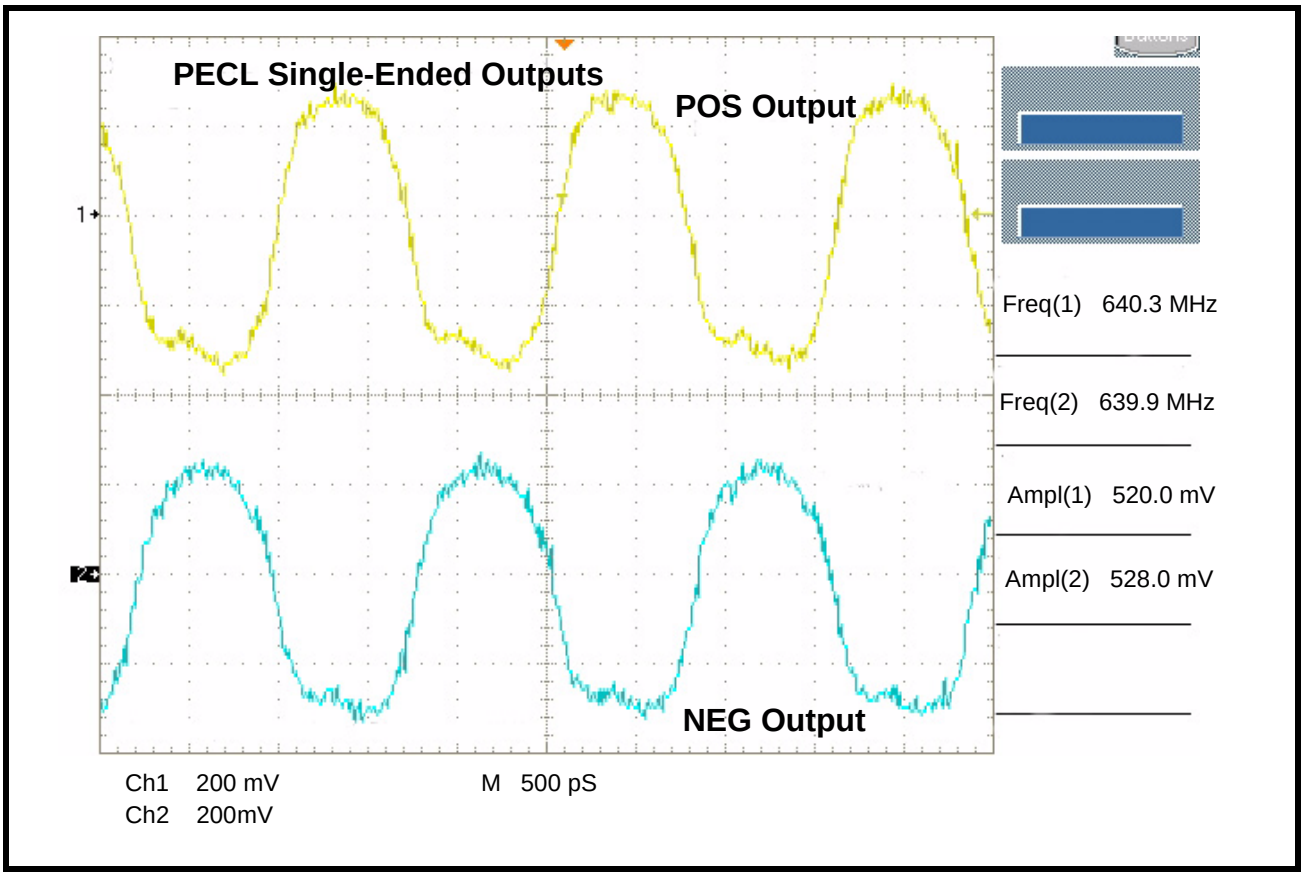


FIGURE 8. PECL SINGLE-ENDED OUTPUTS (POSITIVE AND NEGATIVE OUTPUT REFERENCED TO GROUND)



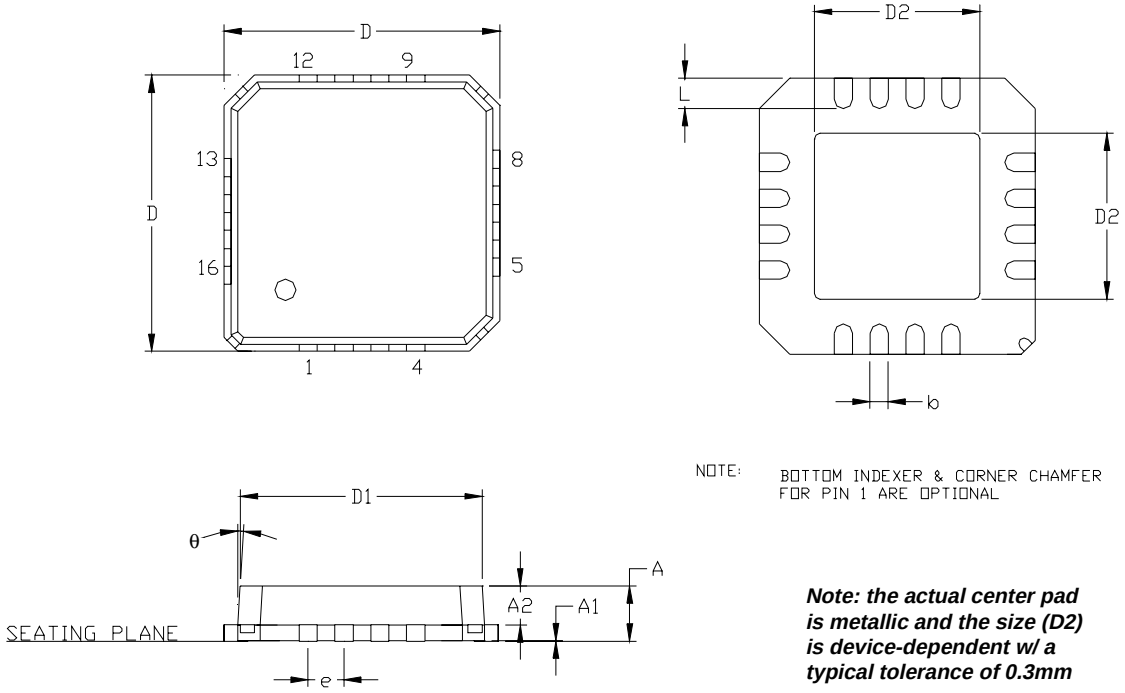
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT8020IL	16-Lead QFN	-40°C to +85°C

PACKAGE DIMENSIONS

16 LEAD QUAD FLAT NO LEAD
(4 mm x 4 mm, 0.65 pitch QFN)

Rev. 1.01



Note: the actual center pad is metallic and the size (D2) is device-dependent w/ a typical tolerance of 0.3mm

Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A2	0.000	0.039	0.00	1.00
D	0.154	0.161	3.90	4.10
D1	0.144	0.152	3.65	3.85
D2	0.088	0.100	2.24	2.54
b	0.009	0.015	0.23	0.38
e	0.0256 BSC		0.65 BSC	
L	0.014	0.030	0.35	0.75
θ	0°	12°	0°	12°

REVISIONS

P1.0.1 Accumulated output jitter in electrical specs changed from 25 ps @ 624MHz to 20 @ 622Mhz and TBD to 20 ps @312Mhz. Pin 9 has internal a pull-down resistor instead of pull-up. Table 1 FS0 and FS1 bit pattern changed.

P1.0.2 Changed typical jitter to 6ps and changed package to QFN

P1.0.3 Corrected package dimension dimension "e" to 0.65 mm BSC. Updated electrical tables. Added descriptive sections on Calibration, Crystal Selection and Data and Plots.

1.0.0 Final Release. Added intrinsic jitter measurements to the electrical characteristics.

1.0.1 Changed the page numbering. Changed the QLP to QFN in the Features on page 1.

1.0.2 Changed the Package Drawing and Dimensions.

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